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Personal, Indoor and Mobile Radio Communications, 1997. 'Waves of the Year 2 PIMRC '97., The 8th IEEE International Symposium on , Volume: 3 , 1-4 Sep 19
Page(s): 776 -780 vol.3

[\[Abstract\]](#) [\[PDF Full-Text \(500 KB\)\]](#) [IEEE CNF](#)**2 A hybrid wave-pipelined network router***Delgado-Frias, J.G.; Nyathi, J.;*

VLSI, 2001. Proceedings. IEEE Computer Society Workshop on , May 2001
Page(s): 165 -170

[\[Abstract\]](#) [\[PDF Full-Text \(736 KB\)\]](#) [IEEE CNF](#)**3 Analysis and comparison of real-time sine-wave generation for PWM c***Mirkazemi-Moud, M.; Green, T.C.; Williams, B.W.;*

Power Electronics, IEEE Transactions on , Volume: 8 Issue: 1 , Jan 1993
Page(s): 46 -54

[\[Abstract\]](#) [\[PDF Full-Text \(476 KB\)\]](#) [IEEE JNL](#)

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1 System design using wave-pipelining: a CMOS VLSI vector unit

Nowka, K.J.; Flynn, M.J.;

Circuits and Systems, 1995. ISCAS '95., 1995 IEEE International Symposium on Volume: 3 , 30 Apr-3 May 1995

Page(s): 2301 -2304 vol.3

[\[Abstract\]](#) [\[PDF Full-Text \(392 KB\)\]](#) **IEEE CNF**

2 Double pass-transistor logic for high performance wave pipeline circuit

Parthasarathy, R.S.; Sridhar, R.;

VLSI Design, 1998. Proceedings., 1998 Eleventh International Conference on , 4 1998

Page(s): 495 -500

[\[Abstract\]](#) [\[PDF Full-Text \(640 KB\)\]](#) **IEEE CNF**

3 Design and realization of high-performance wave-pipelined 8x8 b mul in CMOS technology

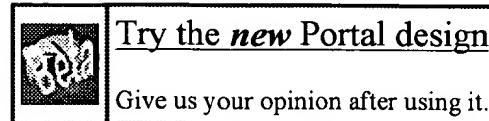
Ghosh, D.; Nandy, S.K.;

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 3 1 , Mar 1995

Page(s): 36 -48

[\[Abstract\]](#) [\[PDF Full-Text \(1004 KB\)\]](#) **IEEE JNL**

4 A bipolar p pulation c unter using wave pipelining to achieve 2.5x no cl ck frequency



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1 Fast detection of communication patterns in distributed executions 84%



Thomas Kunz , Michiel F. H. Seuren

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Understanding distributed applications is a tedious and difficult task. Visualizations based on process-time diagrams are often used to obtain a better understanding of the execution of the application. The visualization tool we use is Poet, an event tracer developed at the University of Waterloo. However, these diagrams are often very complex and do not provide the user with the desired overview of the application. In our experience, such tools display repeated occurrences of non-trivial commun ...

2 Reconfigurable computing: a survey of systems and software 83%



Katherine Compton , Scott Hauck

ACM Computing Surveys (CSUR) June 2002

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Due to its potential to greatly accelerate a wide variety of applications, reconfigurable computing has become a subject of a great deal of research. Its key feature is the ability to perform computations in hardware to increase performance, while retaining much of the flexibility of a software solution. In this survey, we explore the hardware aspects of reconfigurable computing machines, from single chip architectures to multi-chip systems, including internal structures and external coupling. W ...

3 Exploiting FPGA-features during the emulation of a fast reactive embedded system 82%



Karlheinz Weiß , Thorsten Steckstor , Gernot Koch , Wolfgang Rosenstiel

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Kenneth J. Thurber , Leon D. Wald

ACM C mputing Surveys (CSUR) December 1975

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1 Logic cell emulation for ASIC in-circuit emulators

Cravatta, S.J.;

ASIC Seminar and Exhibit, 1990. Proceedings., Third Annual IEEE , 17-21 Sept. 1990

Pages:P5/2.1 - P5/2.4

[Abstract] [PDF Full-Text (260 KB)] IEEE CNF

2 EmGen-a module generator for logic emulation applications

Wen-Jong Fang; Wu, A.C.-H.; Duan-Ping Chen;

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 7 , Issue: 4 , Dec. 1999

Pages:488 - 492

[Abstract] [PDF Full-Text (116 KB)] IEEE JNL

3 Field-programmable integrated circuits-overview and future trends

El Gamal, A.;

Computer Design: VLSI in Computers and Processors, 1992. ICCD '92. Proceedings., IEEE 1992 International Conference on , 11-14 Oct. 1992

Pages:2

[Abstract] [PDF Full-Text (24 KB)] IEEE CNF

4 An undergraduate computer engineering rapid systems prototyping design laboratory

Hamblen, J.O.; Owen, H.L.; Yalamanchili, S.; Binh Dao;

Education, IEEE Transactions on , Volume: 42 , Issue: 1 , Feb. 1999

Pages:8 - 14

[Abstract] [PDF Full-Text (112 KB)] IEEE JNL

5 Using physics based models in virtual reality for dynamic emulation of robotic systems

Li, Y.F.; Wang, J.G.; Ho, J.K.L.;

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1 A partitioning algorithm for technology-mapped designs on single-chip emulation systems

Ejnioui, A.; Ranganathan, N.;

Very Large Scale Integration (VLSI) Systems, IEEE Transactions on , Volume: 9 , Issue: 2 , April 2001

Pages:407 - 410

[\[Abstract\]](#) [\[PDF Full-Text \(96 KB\)\]](#) **IEEE JNL**

2 Logic cell emulation for ASIC in-circuit emulators

Cravatta, S.J.;

ASIC Seminar and Exhibit, 1990. Proceedings., Third Annual IEEE , 17-21 Sept. 1990

Pages:P5/2.1 - P5/2.4

[\[Abstract\]](#) [\[PDF Full-Text \(260 KB\)\]](#) **IEEE CNF**

3 A graphic MMI emulator project for PCs

Popovici, D.;

Frontiers in Education Conference, 2000. FIE 2000. 30th Annual , Volume: 1 , 18-21 Oct. 2000

Pages:F1E/18 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(104 KB\)\]](#) **IEEE CNF**

4 Real-time emulation of indoor multipath propagation channels using statistical and deterministic FIR models and acoustic charge transport technology

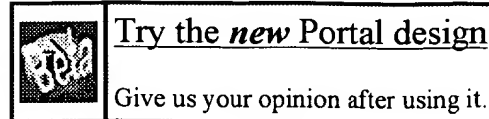
Vigil, A.;

Vehicular Technology Conference, 1993 IEEE 43rd , 18-20 May 1993

Pages:223 - 226

[\[Abstract\]](#) [\[PDF Full-Text \(372 KB\)\]](#) **IEEE CNF**

5 Program emulation in a personal computer: is it really worth it?



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- 1 VLSI circuits: A pipelined clock-delayed domino carry-lookahead adder** 82%


 Bhushan A. Shinkre , James E. Stine

Proceedings of the 13th ACM Great Lakes Symposium on VLSI April 2003

Clock-delayed (CD) domino is a dynamic logic family developed to provide both inverting and non-inverting logic on single-rail gates. It is self-timed and can be easily pipelined for superior speed performance which makes it an attractive option in high-speed logic implementation. This paper presents the design of two different high-speed pipeline configurations of a 32-bit carry look-ahead adder using CD domino gates utilizing efficient clocking methodology to reduce the overall critical path delay ...
- 2 Valid clocking in wavepipelined circuits** 80%


 William K. C. Lam , Robert K. Brayton , Alberto L. Sangiovanni-Vincentelli

Proceedings of the 1992 IEEE/ACM international conference on Computer-aided design November 1992
- 3 Session 7: embedded system techniques (2): Wave pipelining for application-specific networks-on-chips** 77%

 Jiang Xu , Wayne Wolf

Proceedings of the international conference on Compilers, architecture, and synthesis for embedded systems October 2002

This paper presents methods for optimizing application-specific networks-on-chips (NoCs). We show that wave pipelining provides more energy efficient data transport than non-wave pipelined communication. We observe 52% energy saving, 60% transistor area saving, and 1.7 times speedup by using wave pipelining in simulation. Wave pipelining is particularly well suited to networks-on-chips because the network structured interconnection provides better delay control. Our analysis shows how designer ...
- 4 Verifying clock schedules** 77%

 Thomas G. Szymanski , Narendra Shenoy

Proceedings of the 1992 IEEE/ACM international conference on Computer-aided design November 1992

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1 IP validation for FPGAs using Hardware Object Technology™

Casselman, S.; Schewel, J.; Beaumont, C.;

Parallel and Distributed Processing, 1999. 13th International and 10th Symposium on Parallel and Distributed Processing, 1999. 1999 IPSP/SPDP. Proceedings, 12-16 April 1999

Pages:624 - 629

[Abstract] [PDF Full-Text (136 KB)] IEEE CNF

2 A new 'slope-modulated' PWM strategy for implementation in a single chip gate array

Salmon, J.C.;

Industry Applications Society Annual Meeting, 1988., Conference Record of the 1988 IEEE, 2-7 Oct. 1988

Pages:388 - 394 vol.1

[Abstract] [PDF Full-Text (508 KB)] IEEE CNF

3 2003 IEEE MTT-S International Microwave Symposium Digest (Cat. No.03CH37411)

Microwave Symposium Digest, 2003 IEEE MTT-S International, Volume: 2, 8-13 June 2003

[Abstract] [PDF Full-Text (707 KB)] IEEE CNF

4 Telemetry system of daily life motion and arrhythmia

Kobayashi, I.; Hayashi, R.; Sugawara, A.; Matsumoto, H.;

Engineering in Medicine and Biology society, 1997. Proceedings of the 19th Annual International Conference of the IEEE, Volume: 5, 30 Oct.-2 Nov. 1997

Pages:2229 - 2231 vol.5

[Abstract] [PDF Full-Text (220 KB)] IEEE CNF

5 A study on the design and characteristics of the high frequency resonant inverter for ultrasonic motor drive using fuzzy controller

In-Su Cha; Hyeon-Am Park; Gwon-Jong Yu; Young-Dong Kim; Hyung Lae Baek;
Industrial Electronics, Control, and Instrumentation, 1995., Proceedings of the
1995 IEEE IECON 21st International Conference on , Volume: 1 , 6-10 Nov. 1995
Pages:680 - 685 vol.1

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1 Digit-serial design of a wave digital filter

Ming Hu; Vainio, O.; Renfors, M.;

Instrumentation and Measurement Technology Conference, 1999. IMTC/99. Proceedings of the 16th IEEE , Volume: 1 , 24-26 May 1999
Pages:542 - 545 vol.1

[\[Abstract\]](#) [\[PDF Full-Text \(304 KB\)\]](#) IEEE CNF

2 Base/gate drive suppression of inactive power devices of a voltage-fed inverter and precision synthesis of AC voltage and DC link current waves

Joshi, R.P.; Bose, B.K.;

Industrial Electronics Society, 1990. IECON '90., 16th Annual Conference of IEEE , 27-30 Nov. 1990
Pages:1034 - 1040 vol.2

[\[Abstract\]](#) [\[PDF Full-Text \(472 KB\)\]](#) IEEE CNF